CLAIMS

1. A programmable gain voltage buffer comprising:

a gain stage; and

a programmable resistance in communication with the gain stage, the programmable resistance including a switch in parallel with a resistive element.

2. The voltage buffer of claim 1, further comprising:

an output node coupled between the gain stage and the programmable resistance,

wherein the switch is operable to change a gain at the output node.

3. The voltage buffer of claim 2, wherein the gain at the output node has a first gain value when the switch is activated and a second gain value when the switch is deactivated.

4. The voltage buffer of claim 2, wherein the gain is proportional to an equivalent resistance at the output node.

5. The voltage buffer of claim 2, wherein the switch is operable to change the gain in response to being activated and deactivated.

6. The voltage buffer of claim 1, wherein the switch provides a first resistance value in parallel with the resistive element when activated and is effectively removed from the circuit when deactivated.

7. The voltage buffer of claim 6, wherein the first resistance value comprises a source-drain resistance of the switch.

8. The voltage buffer of claim 6, wherein the first resistance value of the switch corresponds to a programmable gain step for the circuit.

9. The voltage buffer of claim 1, wherein the voltage buffer comprises a differential voltage buffer including two branches, each branch including

a gain stage, and

a programmable resistance in communication with the gain stage, the programmable resistance including a switch in parallel with a resistive element

10. The voltage buffer of claim 9, wherein the switches in the two branches are operative to be activated and deactivated substantially simultaneously.

11. The voltage buffer of claim 2, wherein the programmable resistance further comprises:

a second switch in parallel with said switch and the resistive element, the second switch operative to change the gain in response to being activated and deactivated.

12. The voltage buffer of claim 1, further comprising a second circuit operative to control an accuracy of the gain.

13. The voltage buffer of claim 12, wherein the second circuit comprises:

a reference resistive element;

a tunable resistive element in parallel with the reference resistive element, the tunable resistive element operative to track a resistance of the reference resistive element and having a gate with a bias voltage; and

an output line coupled to the gate of the tunable resistive element and a gate of each of the switches.

14. A method comprising:

applying an input signal to a voltage buffer;

activating one or more selected switches in parallel with a predominant resistive element in the voltage buffer; and

changing a gain of the buffer by at least a programmable gain step.

15. The method of claim 14, wherein said changing the gain comprises changing an equivalent resistance at an output point in the voltage buffer.

16. The method of claim 14, further comprising:

deactivating one or more of said selected switches in parallel with the predominant resistive element in the voltage buffer; and

changing a gain of the buffer by at least a programmable gain step.

17. The method of claim 14, wherein said applying the input signal comprises receiving a signal from a first circuit.

18. The method of claim 17, further comprising:

providing an output signal to a second circuit.

19. The method of claim 18, wherein the first circuit comprises a reference voltage circuit.

20. The method of claim 19, wherein the second circuit comprises a load circuit.

21. A device comprising:

a first circuit operative to provide a voltage signal;

a second circuit;

a voltage buffer coupled between the first and second circuits and operative to provide a programmable gain to the voltage signal, the voltage buffer comprising:

a gain stage; and

a programmable resistance in communication with the gain stage, the programmable resistance including a switch in parallel with a resistive element.

22. The device of claim 21, further comprising:

an output node coupled between the gain stage and the programmable resistance,

wherein the switch is operable to change a gain at the output node.

23. The device of claim 22, wherein the gain at the output node has a first gain value when the switch is activated and a second gain value when the switch is deactivated.

24. The device of claim 22, wherein the gain is proportional to an equivalent resistance at the output node.

25. The device of claim 22, wherein the switch is operable to change the gain in response to being activated and deactivated.

26. The device of claim 21, wherein the switch provides a first resistance value in parallel with the resistive element when activated and is effectively removed from the circuit when deactivated.

27. The device of claim 26, wherein the first resistance value comprises a source-drain resistance of the switch.

28. The device of claim 26, wherein the first resistance value of the switch corresponds to a programmable gain step for the circuit.

29. The device of claim 21, wherein the comprises a differential voltage buffer including two branches, each branch including

a gain stage, and

a programmable resistance in communication with the gain stage, the programmable resistance including a switch in parallel with a resistive element

30. The device of claim 29, wherein the switches in the two branches are operative to be activated and deactivated substantially simultaneously.

31. The device of claim 22, wherein the programmable resistance further comprises:

a second switch in parallel with said switch and the resistive element, the second transistor operative to change the gain in response to being activated and deactivated.

32. The device of claim 21, further comprising a second circuit operative to control an accuracy of the gain.

33. The device of claim 32, wherein the second circuit comprises:

a reference resistive element;

a tunable resistive element in parallel with the reference resistive element, the tunable resistive element operative to track a resistance of the reference resistive element and having a gate with a bias voltage; and

an output line coupled to the gate of the tunable resistive element and a gate of each of the switch.

34. A programmable gain voltage buffer comprising:

a gain stage; and

means for providing a programmable resistance in communication with the gain stage, the programmable resistance including switching means in parallel with resistive means.

35. The voltage buffer of claim 34, further comprising:

an output node coupled between the gain stage and the programmable resistance,

wherein the switching means includes means for changing a gain at the output node.

36. The voltage buffer of claim 35, wherein the gain at the output node has a first gain value when the switching means is activated and a second gain value when the switching means is deactivated.

37. The voltage buffer of claim 35, wherein the gain is proportional to an equivalent resistance at the output node.

38. The voltage buffer of claim 35, wherein the switching means is operable to change the gain in response to being activated and deactivated.

39. The voltage buffer of claim 34, wherein the switching means provides a first resistance value in parallel with the resistive means when activated and is effectively removed from the circuit when deactivated.

40. The voltage buffer of claim 39, wherein the first resistance value comprises a source-drain resistance of a switch.

41. The voltage buffer of claim 39, wherein the first resistance value of the switching means corresponds to a programmable gain step for the circuit.

42. The voltage buffer of claim 34, wherein the voltage buffer comprises a differential voltage buffer including two branches, each branch including

a gain stage, and

means for providing a programmable resistance in communication with the gain stage, the programmable resistance including switching means in parallel with resistive means

43. The voltage buffer of claim 42, wherein the switching means in the two branches are operative to be activated and deactivated substantially simultaneously.

44. The voltage buffer of claim 35, wherein the programmable resistance further comprises:

a second switching means in parallel with said switching means and the resistive means, the second switching means including means for changing the gain in response to being activated and deactivated.

45. The voltage buffer of claim 34, further comprising a second circuit including means for controlling an accuracy of the gain.

46. The voltage buffer of claim 45, wherein the second circuit comprises:

means for providing a reference resistance;

means for providing a tunable resistance in parallel with the means for providing the reference resistance, the means for providing the tunable resistance including means for tracking a resistance of the reference resistive means and having a gate with a bias voltage; and

an output line coupled to said gate and a gate of each of the switching means.